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The application of an ordered mesoporous silica film to a GaAs device

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Abstract Pseudomorphic high electron mobility transistors (PHEMTs) are promising devices for use in millimeter-wave and optical communications systems due to their excellent high frequency and low-noise performances. In order to further improve the performance of these devices, their gate lengths must be reduced to the technological limit and a small gate resistance must be realized. However, shorter gates result in an increase of short channel effects that limit microwave performance. In order to reduce the gate resistance, T-shaped gates with large cross-sectional areas are required. However, the thickness and dielectric constant of the passivation layer have major impacts on the gate capacitance. In this study, an ordered mesoporous silica film was introduced as a passivation layer between T-gates. Si_3N_4 with a dielectric constant of 7.4 and ordered mesoporous silica with a dielectric constant of 2.48 were used as passivation layers. The Si_3N_4 dielectric layer and the ordered mesoporous silica film were stacked together and the device characteristics were investigated.

Keywords Ordered mesoporous silica · PHEMT device · GaAs device · Passivation layer

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1 Introduction

Recent, far-reaching developments in civil communication technology have created mass consumer markets for radio-frequency (RF) systems. Mobile communications technologies including cellular phones, mobile internet access, and new communication services are likely to impact human society at least as much as personal computers have in the past 20 years. These new communication systems must transmit, process, and receive large amounts of data in very short periods of time in the GHz frequency range. New functional devices that can realize data processing at high speed are under vigorous development, especially for the range between microwave and millimeter-wave (30–300 GHz) [1]. In RF electronics, a wide variety of different semiconductor materials and various transistor types including metal-semiconductor field-effect transistors (MESFET), heterojunction bipolar transistors (HBT), bipolar complementary metal-oxide semiconductors (BiCMOS), and high electron mobility transistors (HEMT) have been developed [2]. Among them, HEMT is the most promising technology that can operate in the submillimeter-wave frequency range because its constitutional materials provide higher electron mobilities, higher saturation velocities, and higher sheet electron densities. This is the third type of transistor following bipolar transistors and metal-oxide-semiconductors (MOS), and can realize low voltage, low consuming power, and high speed large-scale-integration (LSI). HEMTs are being studied in various applications including pseudomorphic HEMT (PHEMT), InP-based HEMT, and metamorphic HEMT [3]. Compared with existing FET compounds, HEMTs have numerous advantages such as high electron mobility, low source resistance, and high interception frequency due to the high electron velocity in high electric fields, high transconductance, and low output conductance [4].

In particular, PHEMTs are promising devices for millimeter-wave and optical communication systems due to their excellent high frequency and low noise performance. Among them, GaAs-based pseudomorphic HEMTs have stimulated great interest for high speed, extremely high frequency, low noise, and high power applications [5]. With the aim of enhancing the performance of PHEMTs, gate length, L_g, has been reduced to the technological limit. However, this scaling process has the drawback that the parasitic gate resistance, r_g, increases proportionally to $1/L_g$, thus deteriorating the transconductance and, consequently, other important figures of merit of the devices including the current gain and noise figure. Accordingly, while decreasing L_g, the value of the parasitic gate resistance must be kept as low as possible [3]. In order to reduce the gate resistance, T-shaped gates with a large cross-sectional area are required. The shape of the T-gate, the gate footprint length, L_g, and the thickness of the passivation have major impacts on the gate capacitance, C_{gs}, which is a key parameter for the RF performance of the device. The wider head of the T-gate decreases the gate resistance, R_g, but at the same time, the gate capacitance increases. Therefore, selection of the width of the T-gate head results in a trade-off between low resistance and low capacitance. The use of recessed geometry to improve device characteristics is also widespread [5]. The parasitic capacitance, which results from dielectric surrounding the T-shaped gate, greatly affects the device RF properties. However, reduction of the dielectric constant of the passivation layer with the same gate length may enhance the RF properties. An ordered mesoporous silica film is a good candidate for reduction of the dielectric constant of the passivation layer, due to its low dielectric constant and easy control of its formation and electrical properties. Since ordered mesoporous silica material was first reported in 1992 [6], it has been commonly studied in low-k MOSFET applications [7–9]. In this work, a hybrid layer consisting of an ordered mesoporous silica film and a Si_3N_4 film was applied instead of a Si_3N_4 passivation layer, and the effects of the hybrid layer possessing lower dielectric properties on the properties of GaAs-PHEMT device were investigated.

2 Experimental procedures

2.1 PHEMT device

Figure 1 shows a cross-section of the PHEMT device using a Si_3N_4 passivation layer. The PHEMT epitaxial structure was grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate and consists of the following layers: 500 nm GaAs buffer, 30 periods of AlGaAs/GaAs superlattice buffer, an undoped $Al_{0.23}Ga_{0.77}As$ buffer, silicon planar doping (1×10^{12} cm^{-2}), a 2 nm $Al_{0.23}Ga_{0.77}As$ spacer, a 12 nm $In_{0.2}Ga_{0.8}As$ channel, a 3.5 nm $Al_{0.23}Ga_{0.77}As$ spacer, silicon planar doping (4.5×10^{12} cm^{-2}), and a 25 nm $Al_{0.23}Ga_{0.77}As$ Schottky contact layer. Finally, a 40 nm thick undoped GaAs cap layer was grown to protect the active layer from oxidation which can cause defects. A AuGe/Ni/Au metal system was used for the source and drain since it has been widely used as an ohmic contact for GaAs-based devices. A Si_3N_4 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) to protect the device and to support the gate. A Ti/Pt/Au metal system was used for the T-shaped gate [5]. After the formation of the T-shaped gate, two types of passive dielectrics were filled between the gate and the Si_3N_4: 270 nm of Si_3N_4 and a combined layer of Si_3N_4 (20 nm)/ordered mesoporous silica film (200 nm)/Si_3N_4 (50 nm). The sole Si_3N_4 layer was used as a reference. Figure 2 shows the calculated dielectric constant of the stacked bi-layer of Si_3N_4 and mesoporous silica as a function of their relative thicknesses. A dielectric constant of 3 was estimated for the combined layer structure mentioned above.

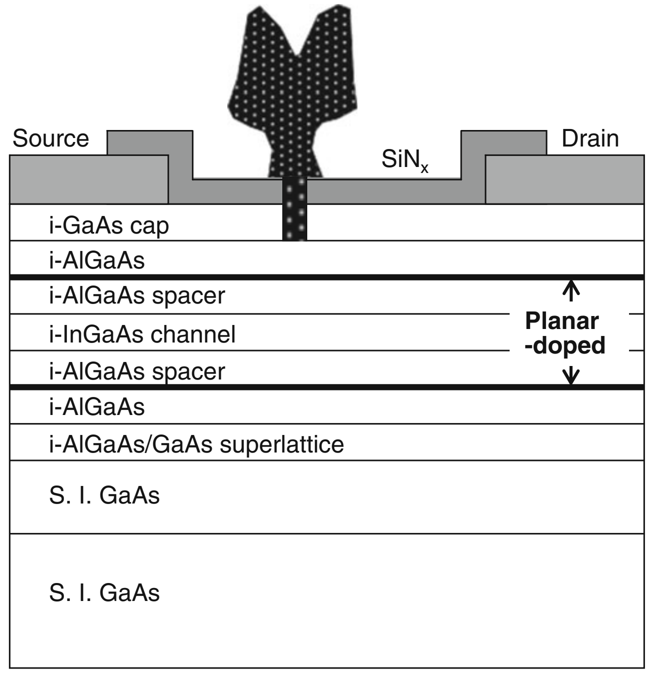

Fig. 1 Cross-sectional view of the PHEMT structure

2.2 Ordered mesoporous silica film

An ordered mesoporous silica film was synthesized using the following processes [10]: silica sol synthesis, spin coating, and calcination. Tetraethoxysilane (TEOS, Fluka Chemica) was used as a silica precursor for the synthesis of ordered mesoporous silica film, and ethanol (EtOH, Duksan Chemical) was used as a solvent. Decaoxyethylene oleyl ether ($C_{18}H_{37}(OCH_2CH_2)_{10}$, Brij-76^R, Aldrich Chemical)

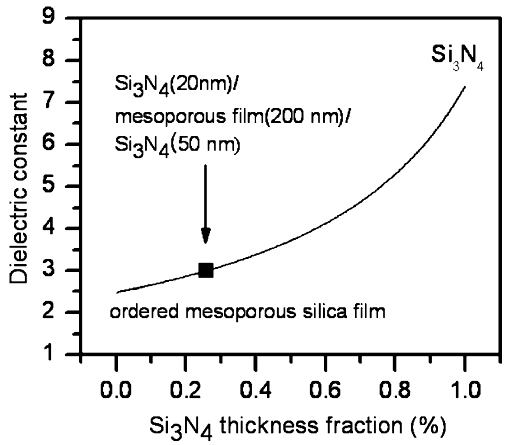

Fig. 2 Theoretical dielectric constant of serial capacitance of the Si_3N_4/ordered mesoporous silica film system. The dielectric constant of Si_3N_4 (20 nm)/ordered mesoporous silica film (200 nm)/Si_3N_4 (50 nm) system is shown as a filled square

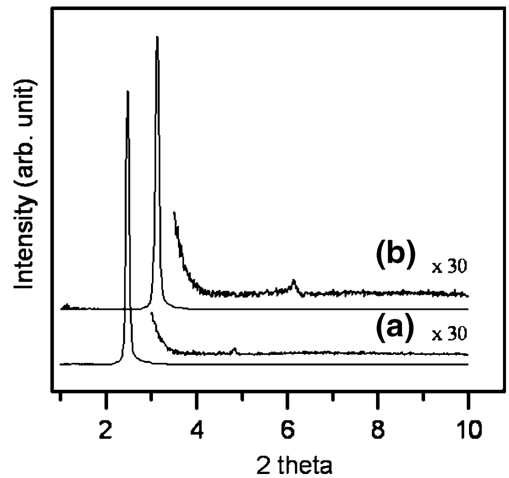

Fig. 3 XRD patterns of (**a**) as-prepared and (**b**) ordered mesoporous silica films

was used as a surfactant. First, TEOS and EtOH were mixed, and then acidified deionized water (DIW) was added for pre-hydrolysis. Separately, Brij-76 block copolymer was dissolved in EtOH and then acidified H_2O was added. After this, the two solutions were mixed for the silica sol. The final molar ratio of TEOS:EtOH:H_2O:HCl: Brij-76 in the solution was 1:20:5:0.01:0.05. Silica sol was spin-coated and a mesoporous silica film was fabricated after calcination at 400°C at a heating rate of 1°C/min. The dielectric constant of the synthesized mesoporous silica film was measured to be 2.48 [11].

3 Results and discussion

Figure 3 shows X-ray diffraction (XRD) patterns of the as-prepared and mesoporous silica films calcined at 400°C. The as-prepared film exhibited a sharp diffraction peak with a plane spacing of 4.49 nm. No other diffraction peaks were observed except for the second harmonic in the magnified XRD pattern shown in Fig. 3(a). Therefore, the as-prepared film exhibited a highly textured pore structure. Even after calcination, the texture characteristics were maintained except for anisotropy shrinkage along the direction normal to the film surface, as shown in Fig. 3(b). The texture characteristics were confirmed by transmission electron microscopy (TEM) observation [11]. Figure 4 shows a TEM image of an ordered mesoporous silica film with a body centered cubic (bcc) pore arrangement where the zone axis was [100].

Figure 5 displays the transconductance and drain current with the gate voltage of the PHEMT device with two differnet types of passive dielectrics: a sole layer of Si_3N_4 (270 nm) and a combined layer of Si_3N_4 (20 nm)/ordered mesoporous SiO_2 (200 nm)/Si_3N_4 (50 nm). As shown in Fig. 5(a), the maximum values of transconductance obtained from the differentiation of the drain current were 499 mS/mm at a gate voltage of -0.25 V for the sole Si_3N_4 layer and 387 mS/mm at a gate voltage of 0.05 V for the combined layer containing mesoporous silica. The maximum transconductance of the combined layer was 22.4% lower that of the sole Si_3N_4 layer. This reduction in the direct current (DC) characteristic was due to the degraded ohmic contact properties resulting from the calcination treatment of the mesoporous silica layer at 400°C.

In general, the DC characteristic is independent of the dielectric properties surrounding the T-gate. However, the RF characteristics depend on the dielectric properties. Typical RF characteristics such as cutoff frequency (f_T) and maximum frequency (f_{max}) were investigated to analyze the effects of the dielectrics to evaluate the usefulness of adopting mesoporous silica as the passive dielectric surrounding the T-gate. For this evaluation, the values of h_{21} and the maximum stable and available gain (MSG/MAG) were measured in the PHEMT devices containing the two different passive dielectrics and the results are given in Fig. 6. The applied gate voltage was determined from the maximum transconductance and this was used to obtain the

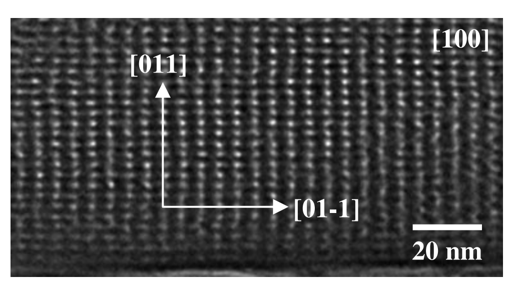

Fig. 4 TEM image of ordered mesoporous silica film with a zone axis of [100]

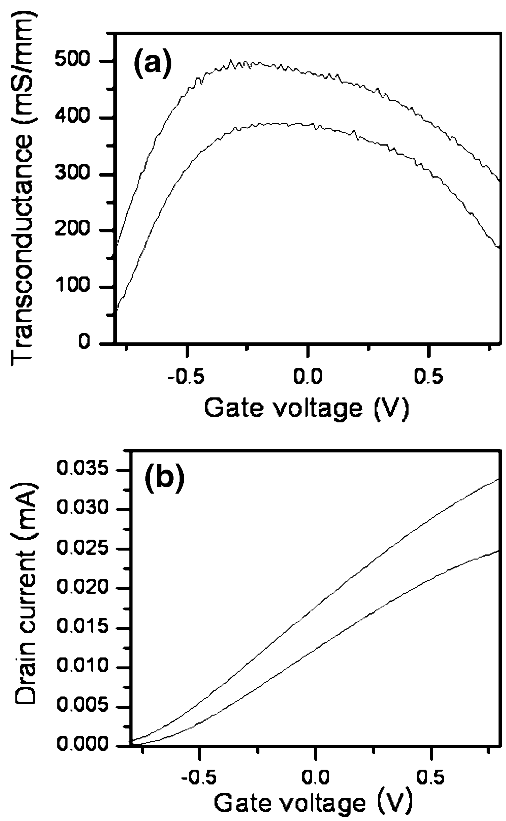

Fig. 5 (**a**) Extrinsic transconductance and (**b**) drain current as a function of the source-to-gate voltage

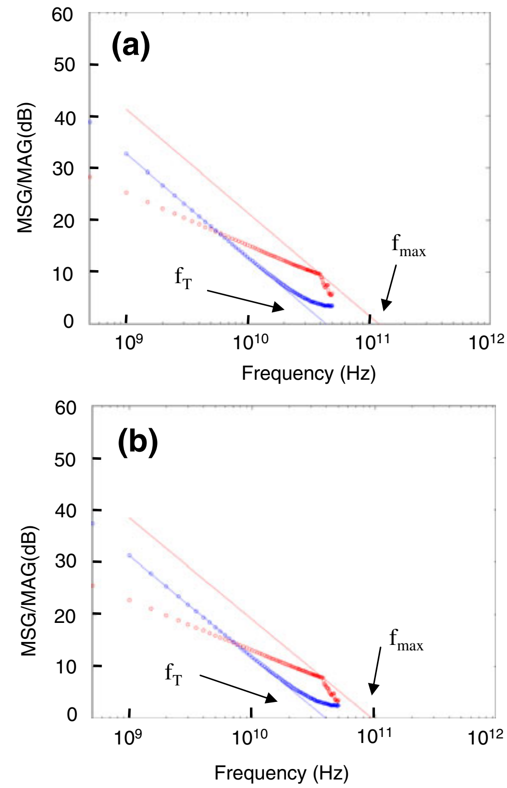

Fig. 6 Measured current gain and maximum available gain as a function of frequency for (**a**) Si_3N_4 (270 nm) and the (**b**) Si_3N_4 (20 nm)/ordered mesoporous silica film (200 nm)/Si_3N_4 (50 nm) system

RF characteristics of the devices. As shown in Fig. 6, the extrapolated f_T and f_{max} were 44.28 GHz and 120.52 GHz at a gate voltage of -0.25 V for the sole Si_3N_4 passive dielectric and 39.81 GHz and 94.07 GHz at a gate voltage of 0.05 V for the combined dielectric, respectively. Considering the DC characteristic, similar property degradation was observed with the combined dielectric. However, as shown in Eq. (1), the cutoff frequency is determined by the capacitance and the DC transconductance between the gate and source where f_T is the current gain cutoff frequency, g_m is the transconductance, C_{gs} is the capacitance between the gate and source, and C_{gd} is the capacitance between the gate and drain.

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \quad (1)$$

As shown in Fig. 5, there was a 22.4% reduction of the DC transconductance for the combined dielectric after calcination treatment at 400°C. However, only a 10% reduction in the cutoff frequency was observed. In other words, the capacitance between the gate and source could be reduced by using the combined dielectric containing mesoporous SiO_2 and it was confirmed that the RF characteristics of the device could be improved. The intrinsic f_T for the combined dielectric could be estimated as 109.37 GHz (2.47 times higher than that of the sole Si_3N_4 passive dielectric) from the direct relation between capacitance and dielectric constant and the independency between transconductance and dielectric. The observed apparent degradation of device properties resulted simply from the calcination treatment which developed pores and masked the device property improvement due to the application of the mesoporous SiO_2. Therefore, if surfactant extraction could be carried out in the micelle structure using the solubility difference of the silica framework and the pore structure can be formed without high temperature calcination, combined dielectrics including mesoporous SiO_2 could be used to improve PHEMT device properties.

4 Conclusions

The application of an ordered mesoporous SiO_2 film was realized in a PHEMT device and its effects were analyzed. Combined dielectric layers of non-porous SiN_x and mesoporous SiO_2 were prepared and compared with a sole SiN_x dielectric layer. However, the DC property of the PHEMT device decreased by 22% due to the possible sinking of the gate metal or Schottky property degradation of ohmic metal due to the high temperature calcination treatment generating pore formation in the mesoporous SiO_2 layer. However, the RF property was only reduced by 10% and it was confirmed that a reduction of capacitance between the gate and source when using a low dielectric material, i.e., mesoporous SiO_2, is important for improving the RF properties of the device. For application of mesoporous SiO_2 to PHEMT devices, it is possible to develop a technique using the concentration difference to extract surfactant instead of applying high temperature calcination treatment.

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